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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,949	11/06/2006	Masato Mori	P30449	8311

52123 7590 10/16/2009

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EXAMINER	
PATEL, DEVANG R	
ART UNIT	PAPER NUMBER
1793	

NOTIFICATION DATE	DELIVERY MODE
10/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/597,949	MORI ET AL.	
	Examiner	Art Unit	
	DEVANG PATEL	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/31/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/1/09 has been entered.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. **Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama et al. (JP 06061636 A) in view of applicant admitted prior art ("AAPA").

a. **Regarding claim 1,** Sakuyama et al. **("Sakuyama")** discloses surface mounting components on a board substrate and specifically discloses separately applying resin and solder powder (i.e. paste) on the board (abstract). Sakuyama teaches first applying only resin on the bond areas 2 of the substrate 1, forming layer 3, and then subsequently applying the solder paste, forming solder layer 4. Thus, the resin is disposed between the paste and bond areas of the substrate. Sakuyama fails to disclose placing components having solder bumps on the applied paste on the circuit substrate and heating the assembly to bond the

components to the substrate. However, such technique is well-known in the art as shown by AAPA.

b. **AAPA** discloses an electronic component mounting method (fig. 10) in which joints between a circuit substrate (21) and electronic components (25/26) are made by placing the components 26 having solder bumps 26a on the printed paste 28 of circuit substrate 21 (fig. 10c) and then heating the assembly to bond the components on the substrate (fig. 10d). Sakuyama discloses surface mount components (which typically have solder bumps) and is not limited to specific type of components. It would have been obvious to a person of ordinary skill in the art at the time of the invention to bond solder-bumped surface mount components similar to AAPA in the method of Sakuyama because such technique (bonding bumped components to applied paste on a substrate) was recognized as part of the ordinary capabilities of one skilled in the art and would have yielded the predictable result of providing reliable joints between the components and the substrate. As the process of Sakuyama in view of AAPA is indistinguishable from the claimed process, it would necessary flow that during the heating step in the method of Sakuyama, the solder paste would flow through the reinforcing resin and contact the bonds areas of the substrate in order to interconnect the substrate and the electronic components.

2. **Alternatively, Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art ("AAPA") in view of Sakuyama et al. (JP 06061636 A).

c. **Regarding claim 1, AAPA** discloses an electronic component mounting method (fig. 10) in which joints between a circuit substrate (21) and electronic components (25/26) are made using solder paste (28). AAPA discloses placing components (26) having solder bumps (26a) on the circuit substrate (fig. 10c) and heating the assembly to bond the components on the substrate (fig. 10d). AAPA discloses printing solder paste on the bond area (fig. 10b), but fails to teach printing the paste on the reinforcing resin such that the resin is between the paste and bond areas of the substrate.

d. **Sakuyama** is drawn to surface mounting components on a board substrate and discloses separately applying resin and solder powder (i.e. paste) on the board (abstract). Sakuyama teaches first applying only resin on the bond areas 2 of the substrate 1, forming layer 3, and then subsequently applying the solder paste, forming solder layer 4. Thus, the resin is disposed between the paste and bond areas of the substrate. Sakuyama discloses that such method obtains sufficient solder layer 4 even on pads 2 having small dimensions and eliminates defective bonding (abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the method of AAPA to supply unhardened resin on the substrate, and then subsequently print the solder paste on the resin similar to Sakuyama in order to eliminate defective bonding even with small pad dimensions. Moreover, the claim would have been obvious because a particular known technique (applying resin and then paste on top) was recognized as part of the ordinary capabilities of one skilled in the art

and would have yielded the predictable result of providing reliable joints between the components and the substrate. As the process of AAPA in view of Sakuyama is indistinguishable from the claimed process, it would necessary flow that during the heating step, the solder paste would flow through the reinforcing resin and contact the bonds areas of the substrate in order to interconnect the substrate and the electronic components.

e. Examiner appreciates that AAPA teaches additional step of applying underfill resin 31 after solder bonding the components. However, the rejection above is not concerned with any subsequent step after bonding the components. More importantly, Examiner points out that the rejection does not substitute the underfill resin of AAPA with the resin of Sakuyama. It is also noted that the present claims do not preclude additional step of applying underfill, wherein the final bonded assembly would contain both the resin of Sakuyama and the underfill resin of AAPA.

3. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama et al. (JP 06061636 A) in view of AAPA OR AAPA in view of Sakuyama as applied to claim 1 above, and further in view of Crane et al. (US 6667194).

f. **As to claim 2,** Sakuyama discloses a resin layer 3, which is equivalent to sheet-form resin as shown in fig. 1b. Nonetheless, **Crane** et al. (drawn to bonding bumped components on a substrate using epoxy resin) discloses a coated sheet resin layer 20 on bond areas 18 of the substrate 16 (fig. 1). It would have been obvious to a person of ordinary skill in the art at the time of the

invention to provide a sheet-form resin similar to Crane in the method of Sakuyama and AAPA since such is an art-recognized alternative form of resin.

g. Neither AAPA nor Sakuyama expressly discloses cooling the resin and the paste. However, such technique is known in the art. After reflow, **Crane** discloses cooling the assembly, thereby solder-bonding the components on the substrate, and hardening (curing) the resin (col. 34, lines 7-17). It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform cooling subsequent to reflow step as shown by Crane in the method of Sakuyama and AAPA because hardening the resin ensures high joint reliability.

4. **Claims 3-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama et al. (JP 06061636 A) in view of AAPA and Crane OR AAPA in view of Sakuyama and Crane as applied to claim 2 above, and further in view of Nakamura et al. (US 6365499).

h. **As to claim 3-5,** none of the references above discloses the sheet-form resin including equally spaced apertures forming a matrix of pores. However, such is also known in the art as shown by Nakamura et al. ("**Nakamura**"). Similar to resin 20 of Crane, Nakamura discloses supplying a sheet-form resin 43 on the circuit substrate 40 (fig. 5B; col. 10, lines 16-20). Nakamura discloses the sheet-form resin including recesses/holes (44) at positions that match the electrode bond areas (42) on the circuit substrate (40- fig. 5c).The claims would have been obvious at the time of the invention because supplying a sheet-form resin having an equally spaced apertures is an art-recognized alternative resin structure. One

skilled in the art would have been motivated to provide the claimed sheet-form resin in the modified bonding method of Sakuyama and AAPA in order to match the metallization patterns on the substrate.

5. **Claims 6-14** are rejected under 35 U.S.C. 103(a) as being obvious over Gonzalez et al. (US 2003/0080437) with supporting evidence of Hayama et al. (US 6051448, of record).

i. **As to claim 6,** Gonzalez et al. ("**Gonzalez**") discloses an electronic component mounting method in which joints are formed between a substrate and electronic components using a reinforcing resin (figs. 6-8). Gonzalez discloses pre-coating the pads 32 (bond areas) of the substrate 30 with a solder paste as known in the art (fig. 8a- step 203; ¶ 30). Although Gonzalez does not expressly disclose "printing" solder paste, the step of pre-coating the paste on one or both surfaces to be joined (bumps and pads) is equivalent to printing. Nonetheless, **Hayama** et al. (drawn to method of manufacturing an electronic component) discloses that it is known to print patterns of paste on a substrate in forming conventional components (col. 1, lines 20-25). Thus, it would have been obvious to print the solder paste in the method of Gonzalez since printing a solder paste on the pads of substrate is a known technique of depositing paste and would have yielded the predictable result of bonding components to one of ordinary skill in the art at the time of the invention. In accordance with broadest reasonable interpretation, the coated/printed solder paste in the method of Gonzalez is restricted in fluidity since the deposited paste layer retains a given shape.

j. Gonzalez further discloses applying a thermosetting reinforcing resin (such as epoxy resin) on the substrate including the solder paste (fig. 8- 205, ¶ 45). Gonzalez then teaches placing the components 130 having solder bumps 132 on the substrate (¶ 49), soldering the components (¶ 53), and hardening the reinforcing resin (fig. 8b).

k. **As to claim 7,** it is reasonable to expect that solder paste would deform during placement of the components since suitable pressure is applied to cause the bumps to physically contact the pads on the substrate (Gonzalez- fig. 8a- step 209).

l. **As to claims 8-10,** Gonzalez discloses drying the solder paste using a heater (reflow - fig. 8b, ¶ 60-62), and such heating intrinsically volatilizes the solvent of the like in the paste.

m. **As to claim 11,** Gonzalez discloses the reinforcing resin being applied on a specified area.

n. **As to claims 12-13,** Gonzalez discloses the resin composition having a flux effect (¶ 57) and an effect of bonding (fig. 8b).

o. **As to claim 14,** the mounted electronic components of Gonzalez are retained by deformation of the solder paste and by adhesive power of the reinforcing resin.

Response to Amendment and Arguments

Applicant's arguments with respect to claims 1 and 6 have been considered but are moot in view of the new ground(s) of rejection. Specifically, Applicant's arguments against the Zhou reference are made in light of the claims as currently amended. The new grounds of rejections under AAPA, Sakuyama, and Gonzalez as set forth above address the amended claims.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 7/31/09 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Conclusion

Claims 1-14 are rejected.

The rejections above rely on the references for all the teachings expressed in the text of the references and/or one of ordinary skill in the art would have reasonably understood from the texts. Only specific portions of the texts have been pointed out to emphasize certain aspects of the prior art, however, each reference as a whole should be reviewed in responding to the rejection, since other sections of the same reference and/or various combinations of the cited references may be relied on in future rejections in view of amendments.

Applicant is reminded to specifically point out the support for any amendments made to the disclosure. See 37 C.F.R. 1.121; 37 C.F.R. Part 41.37; and MPEP 714.02.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVANG PATEL whose telephone number is (571)270-

3636. The examiner can normally be reached on Monday thru Thursday, 8:00 am to 5:30 pm, EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jessica Ward can be reached on 571-272-1223. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. P./
Examiner, Art Unit 1793

/Jessica L. Ward/
Supervisory Patent Examiner, Art Unit 1793